L Number	Hits	Search Text	DB	Time stamp
1	2	"6355524"	USPAT; US-PGPUB	2002/11/22 15:46
3	0	(PVD or (physical adj vapor adj deposition)) same (off with (pedestal adj bias)) same titanium	USPAT; US-PGPUB	2002/11/22 15:52
4	0	(PVD or (physical adj vapor adj deposition)) same (off with (pedestal adj bias))	USPAT; US-PGPUB	2002/11/22 15:51
5	0	(PVD or (physical adj vapor adj deposition)) same (zero with (pedestal adj bias))	USPAT; US-PGPUB	2002/11/22 15:51
6	0	(PVD or (physical adj vapor adj deposition)) same (AC with (pedestal adj bias))	USPAT; US-PGPUB	2002/11/22 15:52
7	0	(PVD or (physical adj vapor adj deposition)) same (pedestal adj bias)	USPAT; US-PGPUB	2002/11/22 15:52
8	0	(PVD or (physical adj vapor adj deposition)) same (off with (pedestal with bias)) same titanium	USPAT; US-PGPUB	2002/11/22 15:52
9	3	(PVD or (physical adj vapor adj deposition)) same (pedestal with bias) same titanium	USPAT; US-PGPUB	2002/11/22 15:57
10	0	(PVD or (physical adj vapor adj deposition)) same (pedestal with bias) same titanium	EPO; JPO; DERWENT; IBM_TDB	2002/11/22 15:55
11	0	(PVD or (physical adj vapor adj deposition)) same (off with AC) same titanium	USPAT; US-PGPUB	2002/11/22 15:56
12	0	(PVD or (physical adj vapor adj deposition)) same (off with AC) same titanium	EPO; JPO; DERWENT; IBM_TDB	2002/11/22 15:56
13	1	(PVD or (physical adj vapor adj deposition)) same (W with AC) same titanium	EPO; JPO; DERWENT; IBM_TDB	2002/11/22 15:57
14	0	(PVD or (physical adj vapor adj deposition)) same (W with AC) same titanium	USPAT; US-PGPUB	2002/11/22 15:57
15	42	(PVD or (physical adj vapor adj deposition)) same (bias) same titanium	USPAT; US-PGPUB	2002/11/22 16:15
16	3	(PVD or (physical adj vapor adj deposition)) same (bias) same titanium	EPO; JPO; DERWENT; IBM_TDB	2002/11/22 16:16
17	0	(PVD or (physical adj vapor adj deposition)) same (AC with power with bias) same titanium	EPO; JPO; DERWENT; IBM_TDB	2002/11/22 16:17
18	1	(PVD or (physical adj vapor adj deposition)) same (AC with power with bias) same titanium	USPAT; US-PGPUB	2002/11/22 16:19
19	5	(PVD or (physical adj vapor adj deposition)) same (AC with power with bias) and (applied adj materials)	USPAT; US-PGPUB	2002/11/22 16:19

US-PAT-NO: 6139699

DOCUMENT-IDENTIFIER: US 6139699 A

TITLE: Sputtering methods for depositing stress tunable tantalum and tantalum nitride films

---------- KWIC ---------

S. M. Rossnagel and J. Hopwood describe a technique which enables control of the degree of directionality in the deposition of diffusion barriers in their paper titled "Thin, high atomic weight refractory film deposition for diffusion barrier, adhesion layer, and seed layer applications" J. Vac. Sci. Technol. B 14(3), May/June 1996. In particular, the paper describes a method of depositing tantalum (Ta) which permits the deposition of the tantalum atoms on steep sidewalls of interconnect vias and trenches. The method uses conventional, non-collimated magnetron sputtering at low pressures, with improved directionality of the depositing atoms. The improved directionality is achieved by increasing the distance between the cathode and the workpiece surface (the throw) and by reducing the argon pressure during sputtering. For a film deposited with commercial cathodes (**Applied Materials** Endura.RTM. class; circular planar cathode with a diameter of 30 cm) and rotating magnet defined erosion paths, a throw distance of 25 cm is said to be approximately equal to an interposed collimator of aspect ratio near 1.0. In the present disclosure, use of this "long throw" technique with traditional, non-collimated magnetron sputtering at low pressures is referred to as "Gamma sputtering".

A process system in which the method of the present invention may be carried out is the **Applied Materials,** Inc. (Santa Clara, Calif.) Endura.RTM. Integrated Processing System. The system is shown and described in U.S. Pat.

No. 5,186,718, the disclosure of which is hereby incorporated by reference.

The preferred embodiments described herein were produced in an Endura.RTM. Integrated Processing System available from **Applied Materials** of Santa Clara, Calif. The **physical vapor deposition** (sputtering in this case) process chamber is capable of processing an 8 inch (200 mm) diameter silicon wafer. The substrate was a silicon wafer having a silicon oxide surface coating with trenches in the surface of the silicon oxide. Sputtering was carried out using a tantalum target cathode having approximately a 35.3 cm (14 in.) diameter, and DC power was applied to this cathode over a range from about 1 kW to about 18 kW. The substrate was placed at a distance of about 25 cm (9.8 in.) from the tantalum target cathode in the case of gamma sputtering, and at a distance of about 14 cm (5.5 in.) from the cathode in the case of IMP sputtering. During IMP sputtering, an **AC bias power** ranging from about 0 W to about 400 W was applied to the substrate, to produce a substrate offset **bias** ranging from about 0 V to about -100 V. The substrate offset **bias** attracts ions from the plasma to the substrate.

DOCUMENT-IDENTIFIER: US 20020070375 A1

TITLE: Stress tunable tantalum and tantalum nitride films

---------- KWIC ---------

Patent Counsel **Applied Materials,** Inc. P.O. Box 450 A Santa Clara CA 65052 US

[0006] S. M. Rossnagel and J. Hopwood describe a technique which enables control of the degree of directionality in the deposition of diffusion barriers in their paper titled "Thin, high atomic weight refractory film deposition for diffusion barrier, adhesion layer, and seed layer applications" J. Vac. Sci. Technol. B 14(3), May/June 1996. In particular, the paper describes a method of depositing tantalum (Ta) which permits the deposition of the tantalum atoms on steep sidewalls of interconnect vias and trenches. The method uses conventional, non-collimated magnetron sputtering at low pressures, with improved directionality of the depositing atoms. The improved directionality is achieved by increasing the distance between the cathode and the workpiece surface (the throw) and by reducing the argon pressure during sputtering. For a film deposited with commercial cathodes (**Applied Materials** Endura.RTM. class; circular planar cathode with a diameter of 30 cm) and rotating magnet defined erosion paths, a throw distance of 25 cm is said to be approximately equal to an interposed collimator of aspect ratio near 1.0. In the present disclosure, use of this "long throw" technique with traditional, non-collimated magnetron sputtering at low pressures is referred to as "Gamma sputtering".

[0035] A process system in which the method of the present invention may be carried out is the **Applied Materials,** Inc. (Santa Clara, Calif.) Endura.RTM. Integrated Processing System. The system is shown and described in U.S. Pat. No. 5,186,718, the disclosure of which is hereby incorporated by reference.

[0040] The preferred embodiments described herein were produced in an Endura.RTM. Integrated Processing System available from **Applied Materials** of Santa Clara, Calif. The **physical vapor deposition** (sputtering in this case) process chamber is capable of processing an 8 inch (200 mm) diameter silicon wafer. The substrate was a silicon wafer having a silicon oxide surface coating with trenches in the surface of the silicon oxide. Sputtering was carried out using a tantalum target cathode having approximately a 35.3 cm (14 in.) diameter, and DC power was applied to this cathode over a range from about 1 kW to about 18 kW. The substrate was placed at a distance of about 25 cm (9.8 in.) from the tantalum target cathode in the case of gamma sputtering, and at a distance of about 14 cm (5.5 in.) from the cathode in the case of IMP sputtering. During IMP sputtering, an **AC bias power** ranging from about 0 W to about 400 W was applied to the substrate, to produce a substrate offset **bias** ranging from about 0 V to about -100 V. The substrate offset **bias** attracts ions from the plasma to the substrate.

US 20020070375A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2002/0070375 A1**

Chiang et al. (43) **Pub. Date: Jun. 13, 2002**

(54) **STRESS TUNABLE TANTALUM AND TANTALUM NITRIDE FILMS**

(76) Inventors: **Tony Chiang**, Mountain View, CA (US); **Peijun Ding**, San Jose, CA (US); **Barry L. Chin**, Saratoga, CA (US)

Correspondence Address:
Patent Counsel
Applied Materials, Inc.
P.O. Box 450 A
Santa Clara, CA 65052 (US)

(21) Appl. No.: **10/060,827**

(22) Filed: **Jan. 29, 2002**

Related U.S. Application Data

(60) Continuation of application No. 09/611,624, filed on Jul. 7, 2000, which is a division of application No. 08/863,451, filed on May 27, 1997, now patented.

Publication Classification

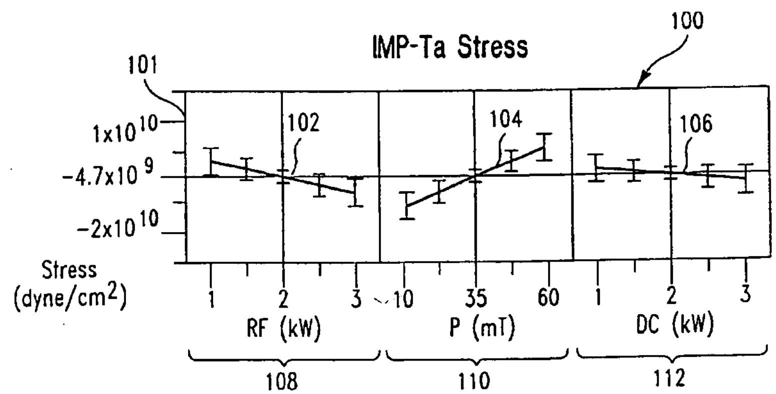
(51) **Int. Cl.**[7] **C23C 14/32**; H01B 1/08

(52) **U.S. Cl.** **252/512**; 204/192.15; 204/192.17; 204/192.21; 252/518.1

(57) **ABSTRACT**

The present disclosure pertains to our discovery that the residual stress residing in a tantalum (Ta) film or a tantalum nitride (TaN_x, where $0<x\leqq1.5$) film can be controlled (tuned) by controlling particular process variables during deposition of the film. Process variables of particular interest during film deposition, for sputter applied Ta and TaN_x films, include the following. The power to the sputtering target; the process chamber pressure (i.e. the concentration of various gases and ions present in the chamber); the substrate DC offset bias voltage (typically an increase in the AC applied substrate bias power); and, the temperature of the substrate upon which the film is being deposited. When the Ta or TaN_x film is deposited using IMP sputtering, the power to the ionization coil can be used for stress tuning of the film. Of these variables, the process chamber pressure and the substrate offset bias most significantly affect the tensile and compressive stress components, respectively. The most advantageous tuning of a sputtered film is achieved using Ion Metal Plasma (IMP) as the film deposition method. This sputtering method provides for particular control over the ion bombardment of the depositing film surface. Tantalum (Ta) films deposited using the IMP method typically exhibit a residual stress ranging from about $+1\times10^{+10}$ dynes/cm^2 (tensile stress) to about $-2\times10^{+10}$ dynes/cm^2 (compressive stress), depending on the process variables described above. Tantalum nitride (TaN_x) films deposited using the IMP method typically can be tuned to exhibit a residual stress within the same range as that specified above with reference to Ta films. We have been able to reduce the residual stress in either the Ta or TaN_x films to range between about $6\times10^{+9}$ and about $-6\times10^{+9}$ dynes/cm^2 using tuning techniques described herein.

The Ta and TaN_x films can also be tuned subsequent to deposition using ion bombardment of the film surface and annealing of the deposited film.



US-PAT-NO: 6093966

DOCUMENT-IDENTIFIER: US 6093966 A

TITLE: Semiconductor device with a copper barrier layer and formation thereof

---------- KWIC ---------

FIG. 7 is a cross-sectional view of an embodiment of the semiconductor device of the present invention after performing even further step(s) in the method of forming such device. In FIG. 7, a copper barrier layer 200 is deposited on the second oxide layer 190 and the insulating layer 180 and along the sidewalls of the opening 195 and 196. The copper barrier layer 200 is typically a tantalum silicon nitride layer, but may also be composed of any combination of refractory metal such as molybdenum, tungsten, **titanium,** vanadium together with silicon and nitrogen (e.g. a nitrogen-containing tantalum). The copper barrier layer 200 is formed on the device of FIG. 6 by an ICP **PVD** process, e.g. using the apparatus shown in prior art FIG. 2, by first providing a plurality of refractory metal atoms and a plurality of silicon atoms in the processing chamber such as the chamber of FIG. 2. Then the atoms are ionized in the chamber, such as the vacuum chamber 35 of prior art FIG. 2, by applying a first **bias** (e.g. by coupling an RF source to the refractory metal and silicon atoms which have been sputtered off the target) to form a plasma containing the atoms, silicon and nitrogen. The refractory metal can be a material selected from the group of tantalum, **titanium,** vanadium, molybdenum, or tungsten. This ionizing step would be processed in an ICP apparatus such as that of prior art FIG. 2. The RF power 50 is applied through coils 55 in prior art FIG. 2. After the atoms are ionized in the processing chamber, the substrate 170, or even the substrate 100 of FIG. 3, is biased with respect to the plasma by application of a two-staged RF power **bias** to accelerate the ionized refractory

metal and silicon atoms to the substrate 170 to form the copper barrier layer 200. As such, the **bias** may be adjusted in two stages. During a first stage **bias** of deposition, which forms the copper barrier layer 200, the first stage **bias** can be kept close to zero, so that no acceleration of ions into the substrate is obtained at this stage. During a second stage **bias**, which forms the copper barrier layer 201 of FIG. 8, the **bias** can be turned on. The first stage **bias** is typically less than the second stage **bias**.

DOCUMENT-IDENTIFIER: US 20020016635 A1

TITLE: Implant with composite coating

---------- KWIC ---------

[0037] FIG. 5 depicts an arc evaporation **physical vapor deposition** apparatus and method for coating a structured surface on a substrate. A water cooled chamber 510 functions as an anode. A vacuum pump 520 and a conduit 530 for a neutral gas and a reactive gas are connected to the chamber 510. The chamber includes a plurality of evaporators 540 that function as cathodes. Each of the evaporators includes a source of a material 545 from which the coating is to be formed (e.g., **titanium**). An arc power supply 550 can be connected to each of the plurality of evaporators 540 (only a single connection is shown in FIG. 5). Each of the evaporators 540 can generate a plasma 560 that includes a high number of ions together with electrons and neutral vapor atoms. (It should be noted that the plasma 560 is represented schematically for clarity.) The plasma 560 impinges upon a substrate 570 that is connected to a **bias** (-) power supply. By increasing the **bias,** the ions are accelerated toward the substrate more rapidly. The apparatus can also include one, or more, structures to steer and/or filter the plasma such as, for example internal and/or external magnets.

DOCUMENT-IDENTIFIER: US 20020171146 A1

TITLE: Compound structure for reduced contact resistance

---------- KWIC ---------

[0049] For one embodiment, the **PVD** process is an IMP process using a **titanium** target, a **bias** power of approximately 0-500 W, a coil power of approximately 100-3000 W, a nitrogen (N.sub.2) flow rate of approximately 5-25 sccm, an argon (Ar) flow rate of approximately 10-50 sccm, and a deposition time of approximately 3-10 seconds. For a further embodiment, the **PVD** process is an IMP process using a **titanium** target, a **bias** power of approximately 300 W, a coil power of approximately 2800 W, a nitrogen flow rate of approximately 13 sccm, an argon flow rate of approximately 40 sccm, and a deposition time of approximately 6 seconds. For alternate embodiments, the nitrogen flow can be replaced by other impurities, such as oxygen or boron flows, to react these impurities with the refractory metal during deposition.

DOCUMENT-IDENTIFIER: US 20020132473 A1

TITLE: Integrated barrier layer structure for copper contact level metallization

---------- KWIC ---------

Patent Counsel **Applied Materials,** Inc. 3050 Bowers Avenue P.O. Box 450A Santa Clara CA 95052 US

[0019] FIG. 1 is a schematic representation of a wafer processing system 35 that can be used to perform integrated circuit metallization in accordance with embodiments described herein. The wafer processing system 35 typically comprises process chambers 36, 38, 40, 41, degas chambers 44, load-lock chambers 46, transfer chambers 48, 50, pass-through chambers 52, a microprocessor controller 54, along with other hardware components such as power supplies (not shown) and vacuum pumps (not shown). An example of such a wafer processing system 35 is an ENDURA.RTM. System, commercially available from **Applied Materials,** Inc., Santa Clara, Calif.

[0025] FIG. 2 depicts a schematic cross-sectional view of a sputtering-type physical vapor deposition (PVD) process chamber 36 of wafer processing system 35. An example of such a PVD process chamber 36 is an IMP VECTRA.TM. chamber, commercially available from **Applied Materials,** Inc., Santa Clara, Calif.

[0032] The **PVD** chamber 36 may comprise additional components for improving the deposition of sputtered particles onto the substrate 120. For example, the **PVD** chamber 36 may include a bias power source 124 for biasing the substrate 120. The bias power source 124 is coupled to the pedestal 112 for controlling material layer deposition onto the substrate 120. The **bias power** source 124 is

typically an **AC** source having a frequency of, for example, about 400 kHz.

[0035] FIG. 3 depicts a schematic cross-sectional view of a chemical vapor deposition (CVD) process chamber 38 of wafer processing system 35. Examples of such CVD chambers 38 include TXZ.TM. chambers, WXZ.TM. chambers and PRECISION 5000.RTM. chambers, commercially available from **Applied Materials,** Inc., Santa Clara, Calif.

[0044] FIG. 4 depicts a schematic cross-sectional view of a rapid thermal processor (RTP) chamber 40 of wafer processing system 35. An example of a RTP chamber 40 is a CENTURA.RTM. chamber, commercially available from **Applied Materials,** Inc., Santa Clara, Calif.

[0064] The above process parameters are suitable for implementation on a 200 mm (millimeter) substrate in a deposition chamber available from **Applied Materials,** Inc., Santa Clara, Calif. Other deposition chambers are within the scope of the invention, and the parameters listed above may vary according to the particular deposition chambers used to form the silicide layer as well as the one or more barrier layers. For example, other deposition chambers may have a larger (e. g., chambers configured to accommodate 300 mm substrates) or a smaller volume, requiring gas flow rates, or powers that are larger or smaller than those recited for deposition chambers available from **Applied Materials,** Inc.

DOCUMENT-IDENTIFIER: US 20010050220 A1

TITLE: METHOD AND APPARATUS FOR PHYSICAL VAPOR DEPOSITION USING MODULATED POWER

---------- KWIC ---------

[0005] To obtain deposition in the high aspect ratio (HAR) features, one method uses a medium/high pressure **physical vapor deposition (PVD**) process known as an ionized metal plasma (IMP) process or high-density plasma **physical vapor deposition** (HDP**-PVD**). The plasma density in such high density plasma processes is typically between about 10.sup.11 cm.sup.-3 and 10.sup.12 cm.sup.-3. Generally, IMP processing offers the benefit of highly directional deposition with good bottom coverage in HAR features. High density plasma sputtering processes have been successfully implemented for obtaining conformal coverage for **titanium** (Ti), **titanium** nitride (TiN), tantalum (Ta), tantalum nitride (TaN), copper (Cu), tungsten (W), and tungsten nitride (WN). In one high density plasma deposition configuration, a typical chamber includes a coil, or other electromagnetic field generating device, for maintaining a high density, inductively-coupled plasma between a target and a susceptor on which a substrate is placed for processing. Initially, a plasma is generated by introducing a gas, such as helium or argon, into the chamber and then coupling energy into the chamber via the target to ionize the gas. The coil is positioned proximate to the processing region of the chamber and produces an electromagnetic field that induces currents in the plasma resulting in an inductively-coupled medium/high density plasma between the target and the susceptor. The ions and electrons in the plasma are accelerated toward the target by the negative **bias** applied to the target causing the sputtering of material from the target. At least a portion of the sputtered metal flux is then ionized by interaction with the plasma. An electric field due to an

applied or self**-bias,** develops in the boundary layer, or sheath, between the plasma and the substrate and electrically attracts and accelerates the metal ions towards the substrate in a direction parallel to the electric field and perpendicular to the substrate surface. The **bias** energy is preferably controlled by the application of power, such as RF or DC power, to the susceptor to attract the sputtered target ions in a highly directionalized manner to the surface of the substrate to fill the features formed on the substrate.

US-PAT-NO: 6443743

DOCUMENT-IDENTIFIER: US 6443743 B1

TITLE: Method for reducing via resistance in small high aspect ratio holes filled using aluminum extrusion

---------- KWIC ---------

The **titanium** film 7 is deposited to provide a good bottom coverage (e.g. >15 to 20 angstroms for films of thickness about 500 angstroms) using either a **PVD** technique (long-throw sputtering, collimated sputtering, ionized metal **PVD** or the like) or a CVD technique. The requirement of the bottom coverage is determined by the amount of **titanium** required to form a co-alloyed interface with aluminum, and is typically set by measuring the via resistance distributions over several vias or via chains. The **titanium** nitride liner 13 deposited over the **titanium** 7 is preferred to have a low bottom coverage (<10% for 500 angstrom thick films, for example). The intent is to not have any **titanium** nitride (ideally) at the bottom of the via, while still providing enough **titanium** nitride (less than or equal to 25 angtroms) along the sidewalls in order to prevent interaction between the aluminum plug material 11 and the **titanium** liner layer 7 under the **titanium** nitride layer 13. A conventional sputtering techique (without using long-throw, collimation or ionized metal **PVD**) is ideally suited for this purpose. The step coverage can be deliberately degraded both for the conventional sputtering as well as for collimated and ionized **PVD** methods by suitably altering the deposition parameters such as deposition temperature, gas pressure, substrate **bias,** target geometries and coil power. The aluminum plug 11 extends from the metal layer 3 to the metal layer 5 to provide the interconnect.

US-PAT-NO: 6197167

DOCUMENT-IDENTIFIER: US 6197167 B1

TITLE: Step coverage and overhang improvement by pedestal bias voltage modulation

---------- KWIC ---------

However, an applied **bias** to the substrate causes re-sputtering of the deposited material at the top portion of the feature aperture. The amount of re-sputtering increases with the power of the applied **bias** to the substrate The re-sputtered material deposits onto the side walls of the aperture and forms overhangs. This undesirable crowning effect restricts subsequent deposition into the aperture. Because the bottom coverage and the formation of overhangs depends on the **bias** power applied at the surface of the substrate, HDP **PVD** still presents problems when a higher bottom coverage is desired. FIG. 1a is a cross sectional view of a high aspect ratio feature deposited using HDP **PVD** techniques at a high (.apprxeq.400 W) electrostatic chuck **bias,** and FIG. 1b is a cross sectional view of a high aspect ratio feature deposited using HDP **PVD** techniques at a low (.apprxeq.200 W) electrostatic chuck **bias**. Both FIGS. 1a and 1b illustrate deposition of 1000 .ANG. of **titanium** nitride (TiN) on the surface of the substrate. When high **bias** is applied, bottom coverage improves to between 35% and 46% in a high aspect ratio feature having 0.35 .mu.m width and 1.2 .mu.m depth. However, the high **bias** causes re-sputtering of the deposited material from the deposited material near the top edge of the feature to form large overhangs on the side walls near the upper portion of the aperture, which again restricts subsequent deposition. When low **bias** is applied, the overhang formation is minimized, but the bottom coverage decreases

as well because a lesser amount of deposition is directed by the substrate **bias** to the bottom of the feature.

US-PAT-NO: 5783282

DOCUMENT-IDENTIFIER: US 5783282 A

TITLE: Resputtering to achieve better step coverage of contact holes

---------- KWIC ---------

In a third embodiment of the invention, during **PVD** of a material, a substrate **bias** is applied during deposition such that a portion of the deposited material on the contact bottom is resputtered onto contact sidewalls. In the preferred case, **titanium** is the deposited material. A subsequent anneal step in a nitrogen-containing ambient forms a passivating **titanium** nitride film on the sidewalls of the contact. This passivating film protects the underlying substrate from degradation when metal interconnect material is subsequently deposited in the contact hole. By resputtering a portion of the deposited **titanium** onto the sidewalls of the contact hole, chemical vapor deposition of **titanium** nitride is not required to form a **titanium** nitride film on the contact sidewalls. In this embodiment of the invention, any type of deposition is used, such as ion beam, electron beam, and high density plasma sputter deposition among others well known to one skilled in the art. A collimator and the faceting technique of the first and second embodiments of the invention are not needed to accomplish the object of this third embodiment.

In a third embodiment of the invention, as shown in FIGS. 7a and 7b, during **PVD** of a material, a substrate **bias** is applied during deposition such that a portion of the deposited material 712 on the contact bottom 726 is resputtered onto contact sidewalls 740. Sputtering is used to deposit a refractory metal 712, such as **titanium,** tungsten, tantalum, and molybdenum, and to form a

silicided contact. In the preferred case, **titanium** is the deposited material 712. The contact hole 710 is etched into an second material layer 722, overlying a semiconductor substrate 724. The second material 722 typically comprises an oxide, such as silicon dioxide, or another insulating material, such as borophosphosilicate glass (BPSG). A subsequent anneal step in a nitrogen-containing ambient forms a passivating **titanium** nitride film 727 on the sidewalls 740 of the contact hole 710. This passivating film 727 protects the underlying materials 722 and 724 from degradation when metal interconnect material is subsequently deposited in the contact hole 710. By resputtering a portion of the deposited **titanium** 712 onto the sidewalls 740 of the contact hole 710, chemical vapor deposition of **titanium** nitride 727 is not required to form a **titanium** nitride film 727 on the contact sidewalls 740.